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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,409	04/14/2004	Burnell G. West	NPT-65.0405	8168

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EXAMINER

KERVEROS, JAMES C

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 08/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/825,409

Applicant(s)

WEST ET AL.

Examiner

JAMES C. KERVEROS

Art Unit

2138

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 July 2006.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-7, 9-15 and 17-22 is/are rejected.
7) ☒ Claim(s) 8, 16 and 23 is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 14 April 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a FINAL Office Action in response to Amendment filed 7/21/2006, which claims priority of the copending provisional patent application, 60/463,166, filed April 15, 2003. Claims 1-23 are still pending in the Application.

The drawings received on 7/21/2006 are acceptable. Therefore, the prior Office Action objection to the drawings is hereby withdrawn.

Objection to the abstract of the disclosure is hereby withdrawn in view of the amendment to the Abstract.

Objection to the disclosure is hereby withdrawn in view of the amendment to the specification.

Response to Arguments

Applicant's arguments filed 7/21/2006, with respect to claims 1-7, 9-15 and 17-22, have been fully considered but they are not persuasive.

In response to Applicant's argument, page 10, with respect to independent claims 1, 9 and 17, that Wohl describes the generation of a single seed for multiple test patterns, while in contrast Applicant's claimed invention pertains to the selection of one test pattern versus another based on the test results of a preceding test, the Examiner notes that even though Wohl describes the generation of a seed for multiple test patterns, clearly in the Summary of the Invention, Wohl describes that "pattern generation can target as many faults as possible in a single pattern while ensuring that the care bits have compatible values. To improve test application time, the number of scan cells for one pattern, cells-per-pattern, can be selected, thereby providing a high

probability that a seed exists to set the necessary care bits". Wohl further describes that, "other faults can be tested by patterns that share a large number of common scan cell values. The test pattern generation of the embodiments of the present invention can exploit this commonality by creating a single pattern to test all these faults". With respect to Figure 2A Wohl describes, that "during the last stages of testing approximately 240 care bits may be needed to be set within a single pattern". Clearly, Wohl teaches the use of a single pattern to test various faults of a device under test to improve test application time.

Applicant's argument, page 11, with respect to the example of a two step process, in which the first step pertains to generating test patterns and the second step pertains to selecting and using one of the test patterns generated in the first step, the Examiner notes that Applicants argument is not relevant to claimed invention, since the example cited above is not part of the claims. The claimed invention merely recites that, "the second test pattern is selected based on a diagnosis of the anomalous data by the test apparatus".

Applicant argues, page 11, Wohl does not show or suggest selecting a test pattern for a second test based on a diagnosis of test results from a first test. In response to Applicant's argument, clearly, according to Wohl, Figure 3A illustrates an overview of one seed generation process 300, including the steps of: sending a first test pattern (step 302) for starting a new set of patterns to test the faults created in a list (step 301), and selecting a second test pattern (step 303) based on the test results (step 305) received from the DUT in MISR-LFSR 150, where the test results are

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analyzed to determine if a fault is detected. Finally, if more untested faults are present, as determined in step 305, then steps 302-305 are repeated until no untested faults are left. Any time the process is repeated for testing an untested fault, the test flow proceeds to step (step 303), which corresponds to selecting a second test pattern, as shown in more detail in Figure 3B, which describes the step of adding patterns to the set. In step 312, a new test for detecting a fault can be provided to the pattern. If there are remaining untested faults, as determined in step 313, then step 314 can be performed to determine whether the number of care bits set is less than a maximum number of scan cells that can be set for a single seed.

Applicant's arguments, see Remarks, page 11, filed 7/21/2006, with respect to claims 8, 16 and 23 have been fully considered and are persuasive. The rejection of 8, 16 and 23 has been withdrawn, because of allowable subject matter.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7, 9-15 and 17-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Wohl et al. (US 6,950,974), filed: September 7, 2001.

Regarding independent Claims 1, 9, 17, Wohl discloses an apparatus and method of testing an integrated circuit, IC (DUT) 130, by applying multiple test patterns to the inputs of the circuit and monitoring its outputs to detect the occurrence of faults, Figure 2A, comprising:

Sending a first test pattern (step 302) to the device under test (DUT) 130, using a pseudorandom pattern generator (PRPG) circuit, which generates a bit sequence for each of the scan chains (131-136), Figures 1B, 2A and 3A-C.

Evaluating test results (step 305) received from the DUT in MISR-LFSR 150, where the test results are analyzed to determine if a fault is detected, corresponding to anomalous data indicative of a defect in the DUT;

Automatically selecting a second test pattern (step 303) that is not part of the planned sequence of tests in (step 302), wherein the second test pattern is selected based on detected faults the DUT. Referring to Figure 3B, which describes the step of adding patterns to the set (i.e. step 303), a new pattern can be started with no care bits set in step 311. In step 312, a new test for detecting a fault can be provided to the pattern, as indicated in Figure 3C.

Regarding Claims 2, 10, 18, Wohl discloses the anomalous data is saved and evaluated by the test apparatus, using a computer readable program code, which includes computer readable program code that computes multiple tests for each pattern,

wherein each test detects a fault associated with an integrated circuit (IC) design, as well as computer readable program code that computes multiple patterns for each seed.

Regarding Claims 3-6, 11-14, 19-21, Wohl discloses a plurality of pins for receiving signals from the DUT through output scan pins (SO), and for capturing and storing the test results. Scan chain 131 includes an input scan pin (si1) and an output scan pin (so1). Scan chains 132-136 include corresponding scan pins si2/so2, si3/so3, si4/so4, si5/so5, and si6/so6, respectively.

Regarding Claims 7, 15, 22, Wohl discloses second test pattern (step 303) is selected from a plurality of pre-computed test patterns, wherein the second test pattern is selected according to the pattern, as shown in Figure 3B, which describes the step of adding patterns to the set (i.e. step 303), then a new pattern can be started with no care bits set in step 311. In step 312, a new test for detecting a fault can be provided to the pattern, as indicated in Figure 3C.

Allowable Subject Matter

Claims 8, 16 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior arts of record taken alone or in combination fail to teach, anticipate, suggest or render obvious, "recognizing a pattern in said anomalous data, wherein said second test pattern is selected according to said pattern", as recited in claims 8, 16, 23.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

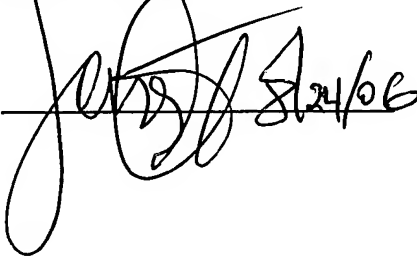
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Date: 24 August 2006
Office Action: Final Rejection

JAMES C KERVEROS
Examiner
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A handwritten signature in black ink, appearing to read 'JCK', is written over a horizontal line. To the right of the signature, the date '8/24/06' is handwritten.